IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A vertical semiconductor device structure, comprising:

a substrate defining a substantially horizontal plane;

a gate electrode projecting vertically from said substrate and including a vertical sidewall;

a spacer flanking said vertical sidewall;

a semiconducting nanotube positioned between said ~~gate electrode~~ vertical sidewall and said spacer and extending between opposite first and second ends with a substantially vertical orientation;

a gate dielectric disposed on said vertical sidewall between said nanotube and said gate electrode;

a source electrically coupled with said first end of said nanotube; and

a drain electrically coupled with said second end of said nanotube.

2. (Original) The semiconductor device structure of claim 1 wherein said source is composed of a catalyst material effective for synthesizing said semiconducting nanotube by a chemical vapor deposition process.

3. (Original) The semiconductor device structure of claim 1 wherein said drain comprises a catalyst material effective for synthesizing said semiconducting nanotube by a chemical vapor deposition process.

4. (Original) The semiconductor device structure of claim 1 wherein said spacer is separated from said substrate by a gap, said gap being filled by an insulating material after said semiconducting nanotube is formed.

5. (Original) The semiconducting device structure of claim 1 wherein said semiconducting nanotube is composed of arranged carbon atoms.

6. (Original) The semiconducting device structure of claim 1 wherein said spacer is separated from said vertical sidewall by a passage.

7. (Original) The semiconducting device structure of claim 6 wherein said passage has horizontal dimensions appropriate for the growth of said semiconducting nanotube and a vertical dimension greater than or equal to a vertical height of said vertical sidewall of said gate electrode.

8. (Original) The semiconducting device structure of claim 6 wherein said passage has a rectangular cross-sectional profile when viewed in a vertical direction.

9. (Original) The semiconducting device structure of claim 6 wherein said source is composed of a catalyst material effective for synthesizing said semiconducting nanotube by a chemical vapor deposition process, said source positioned on said substrate in vertical alignment with said passage.

10. (Original) The semiconducting device structure of claim 9 wherein said spacer is vertically spaced relative to said substrate to define a gap effective for providing a reactant to said catalyst material of said source effective to grow said semiconducting nanotube by a chemical vapor deposition process.

11. (Original) The semiconducting device structure of claim 10 wherein said gap is filled by an insulating material after said semiconducting nanotube is grown by a chemical vapor deposition process.

12. (Original) The semiconducting device structure of claim 6 further comprising a plurality of semiconducting nanotubes positioned horizontally between said gate electrode and said spacer, each of said plurality of semiconducting nanotubes extending vertically in said passage between opposite first and second ends.

13. (Original) The semiconducting device structure of claim 12 wherein space within said passage not occupied by said plurality of semiconducting nanotubes is filled by an insulating material.

14. (Original) The semiconducting device structure of claim 1 further comprising a plurality of semiconducting nanotubes positioned horizontally between said gate electrode and said spacer, each of said plurality of semiconducting nanotubes extending vertically between opposite first and second ends.

15. (Original) The semiconducting device structure of claim 14 wherein at least one of said plurality of semiconducting nanotubes has said first end electrically coupled with said source and said second end electrically coupled with said drain.

16-41. (Cancelled)

42. (New) A semiconductor device structure, comprising:

a substrate;

a gate electrode projecting from said substrate and including a sidewall;

a spacer flanking said sidewall;

a semiconducting nanotube positioned between said sidewall and said spacer and extending between opposite first and second ends;

a gate dielectric disposed on said sidewall between said nanotube and said gate electrode;

a source electrically coupled with said first end of said nanotube; and

a drain electrically coupled with said second end of said nanotube, said gate electrode

being positioned between said drain and said source.

43. (New) The semiconductor device structure of claim 42 wherein said spacer is separated from said substrate by a gap and said spacer is separated from said sidewall by a passage communicating with said gap, said semiconducting nanotube being positioned in said passage, and further comprising:

an insulating material filling said gap and said passage, said insulating material surrounding said semiconducting nanotube within said passage.

44. (New) The semiconductor device structure of claim 42 wherein said spacer is separated from said substrate by a gap, and further comprising:

an insulating material filling said gap.

45. (New) The semiconductor device structure of claim 42 wherein said spacer is separated from said sidewall by a passage, said semiconducting nanotube being positioned in said passage, and further comprising:

an insulating material filling said passage, said insulating material surrounding said semiconducting nanotube within said passage.